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Machine Learning-Based Fault Detection in VLSI Circuits

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Abstract

The rapid advancement of Very Large Scale Integration (VLSI) technology has led to highly complex and densely packed circuits, increasing the probability of faults during manufacturing and operation. Traditional fault detection techniques such as Automatic Test Pattern Generation (ATPG) and fault simulation face significant challenges, including high computational cost, increased test time, and limited scalability for modern nanometer-scale circuits. To address these limitations, this research explores the application of machine learning (ML) techniques for efficient fault detection and localization in VLSI circuits. Various ML algorithms, including Support Vector Machines (SVM), Random Forests, Artificial Neural Networks (ANN), and Graph Neural Networks (GNN), are analyzed for their ability to classify and detect faults based on circuit response data. The proposed framework involves data collection through test patterns, feature extraction, model training, and fault classification. Performance is evaluated using metrics such as accuracy, precision, recall, and F1-score. The study highlights the advantages of ML-based approaches in improving fault detection accuracy, reducing testing time, and enabling scalable solutions. Additionally, it identifies existing research gaps and suggests future directions toward adaptive, real-time, and intelligent testing systems for next-generation VLSI technologies.

Keywords: VLSI Testing, Fault Detection, Machine Learning, Fault Classification, Deep Learning, Fault Localization

Introduction

The continuous advancement of Very Large Scale Integration (VLSI) technology has enabled the integration of millions to billions of transistors on a single chip, forming the backbone of modern electronic systems such as communication devices, automotive electronics, medical equipment, and consumer products. As technology scales down to nanometer dimensions, circuits become increasingly complex, faster, and more power-efficient. However, this rapid growth in integration density also leads to a higher probability of faults arising from manufacturing defects, process variations, aging effects, and environmental disturbances[1, 2].

Fault detection plays a critical role in ensuring the reliability and correct functionality of VLSI circuits. Traditional testing techniques, including Automatic Test Pattern Generation (ATPG), fault simulation, and scan-based testing, have been widely used to detect faults such as stuckat, bridging, and delay faults[3, 4]. Although these deterministic approaches provide high fault coverage for small and medium-scale circuits, they face significant challenges in terms of scalability, computational complexity, and test data volume when applied to modern large-scale systems-on-chip (SoCs)[5].

To overcome these limitations, machine learning (ML) has emerged as a promising data-driven approach for fault detection and classification in VLSI circuits. ML algorithms can learn complex relationships between input test patterns and circuit responses, enabling automatic fault identification without requiring explicit rule-based programming[6].

Classical ML techniques such as Support Vector Machines (SVM), Decision Trees, k-Nearest Neighbors (k-NN), and Random Forests have demonstrated effective performance in structured datasets generated from ATPG simulations[7, 8, 9].

With the increasing complexity of circuits, deep learning methods have gained attention due to their ability to model nonlinear patterns and extract features automatically from large datasets. Artificial Neural Networks (ANNs) and Convolutional Neural Networks (CNNs) have shown improved accuracy in fault detection tasks by reducing dependency on manual feature engineering[10, 11]. Furthermore, recent advancements in Graph Neural Networks (GNNs) enable modeling of circuit topology, providing better fault localization by capturing structural relationships between components[12].

Despite these advancements, several challenges remain. Most existing studies rely heavily on simulated benchmark datasets rather than real silicon validation, limiting their industrial applicability[13]. Additionally, research has primarily focused on simple fault models such as stuck-at faults, while more complex fault types like transient and delay faults are less explored[14]. Moreover, issues related to scalability, generalization across different circuit architectures, and integration with electronic design automation (EDA) tools continue to hinder practical deployment[15].

In this context, this paper presents a comprehensive study of machine learning-based fault detection techniques for VLSI circuits. It aims to analyze and compare traditional and modern approaches, identify existing research gaps, and propose future directions for developing scalable, adaptive, and intelligent testing systems.

Literature Survey

Fault detection in VLSI circuits has been an active area of research due to the increasing complexity of integrated circuits and the need for reliable system performance. Traditional fault detection techniques such as Automatic Test Pattern Generation (ATPG) and fault simulation have been widely used to detect manufacturing defects and operational faults in digital circuits[1, 2]. However, these deterministic approaches face scalability issues when applied to modern nanometer-scale circuits with high transistor density[3].

To overcome these limitations, machine learning (ML) techniques have been introduced for fault detection and classification. Early studies demonstrated the effectiveness of classical ML algorithms such as Support Vector Machines (SVM), Decision Trees, and k-Nearest Neighbors (k-NN) in classifying faults using structured datasets generated from test patterns[4, 5]. Ensemble methods like Random Forest further improved classification accuracy by reducing overfitting and increasing robustness[6].

Recent research has focused on integrating ML with test pattern generation techniques. For instance, hybrid approaches combining ML with Linear Feedback Shift Registers (LFSR) have been proposed to improve test coverage and reduce computational complexity[7]. Similarly, machine learning-assisted ATPG methods have shown promising results in optimizing test vectors and reducing testing time[8].

With advancements in artificial intelligence, deep learning techniques have gained significant attention in VLSI fault detection. Artificial Neural Networks (ANNs) have been widely used to model nonlinear relationships between circuit responses and fault conditions[9]. Convolutional Neural Networks (CNNs) have been successfully applied to analyze structured test response data, enabling automatic feature extraction and improving fault detection accuracy [10]. Advanced architectures such as autoencoders and semi-supervised deep learning models have further enhanced performance by reducing dependency on labeled datasets[11].

In addition, recent studies have explored the use of Graph Neural Networks (GNNs) for modeling circuit topology. GNN-based approaches capture structural relationships between circuit components, leading to improved fault localization and generalization across different circuit architectures[12]. These methods have shown superior performance compared to traditional ML models, particularly in complex and large-scale circuits.

Several recent works have proposed AI-augmented frameworks for fault detection in VLSI circuits, combining multiple ML techniques to enhance detection accuracy and efficiency[13]. For example, deep learning-based models such as temporal convolutional neural networks have been used to detect and localize faults in both analog and digital circuits with high precision[14]. Similarly, semi-supervised learning approaches have been applied for post-silicon fault localization, improving diagnostic capabilities in real-world scenarios[15].

Machine learning techniques have also been extended to analog circuit fault detection, where parametric and soft faults are identified using frequency response analysis and statistical feature extraction[16]. Furthermore, intelligent signal analysis systems based on ML have been developed to automate fault diagnosis in integrated circuits, enabling faster and more reliable testing processes[17].

Recent studies emphasize the importance of data-driven approaches for improving fault detection accuracy and scalability. ML-based frameworks have demonstrated

significant improvements in fault classification performance, achieving high accuracy rates and reducing test time compared to traditional methods[18]. Additionally, ML techniques have been applied to power estimation and reliability analysis in VLSI circuits, further enhancing system performance and fault tolerance[19].

Despite these advancements, several challenges remain in the field. Most existing research relies on simulated benchmark datasets rather than real silicon validation, limiting practical applicability[20]. Moreover, current studies primarily focus on simple fault models such as stuck-at faults, while more complex fault types, including transient and delay faults, are less explored[21]. The lack of standardized datasets and benchmarking frameworks also makes it difficult to compare different approaches objectively[22].

Another key challenge is the high computational requirement of deep learning models, which limits their use in real-time applications[23]. Additionally, the generalization of ML models across different circuit architectures and technology nodes remains an open research problem[24]. To address these issues, recent research has explored hybrid approaches that combine ML with traditional testing methods to improve scalability and efficiency[25].

Overall, the literature indicates a clear transition from traditional deterministic testing methods to intelligent, data driven fault detection approaches. While classical ML models provide efficiency and interpretability, deep learning and graph-based methods offer improved accuracy and scalability for complex VLSI systems. Future research should focus on developing adaptive, real-time, and industry-ready ML frameworks for fault detection in next generation VLSI circuits.

Proposed System Architecture

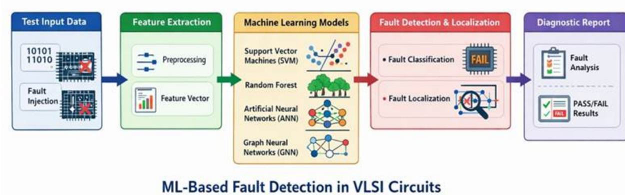

Fig. 1: System Architecture

The system architecture represents a machine learning-based framework for fault detection and localization in VLSI circuits. It consists of multiple stages that process circuit data and generate diagnostic results.

1. Input Data

The first stage includes the input to the system, which consists of:

- VLSI circuit under test
- Test patterns generated using ATPG

These test patterns are applied to the circuit to obtain response data, which contains both fault-free and faulty behavior.

2. Feature Extraction

In this stage, the raw circuit response data is processed to extract meaningful features.

- Data preprocessing is performed
- Important parameters and patterns are converted into feature vectors

This step reduces complexity and prepares the data for machine learning models.

3. ML Model Training & Testing

The extracted features are fed into machine learning algorithms such as:

- Support Vector Machine (SVM)
- Random Forest
- Artificial Neural Networks (ANN) The dataset is divided into training and testing sets: Training: Model learns patterns
- Testing: Model performance is evaluated

4. Fault Classification & Localization

The trained model analyzes new input data to:

- Detect whether a fault is present
- Classify the type of fault
- Identify the location of the fault in the circuit This stage improves speed and accuracy compared to traditional methods.

5. Output Results (Diagnosis Report)

Finally, the system generates output results:

- Diagnostic report
- Fault type and location
- Pass/Fail status

This report helps engineers take corrective actions.

Methodology

The proposed methodology presents a systematic framework for machine learning-based fault detection and localization in VLSI circuits. It consists of multiple stages, starting from circuit selection to deployment of trained models.

A. Circuit Selection and Benchmarking

The first step involves selecting standard benchmark circuits for experimentation. Commonly used benchmark datasets include:

- ISCAS'85 (combinational circuits)
- ISCAS'89 (sequential circuits)
- ITC'99 benchmark circuits

These benchmarks are widely accepted in research and provide predefined fault simulation data. The selected circuits are represented at gate-level or netlist format and are simulated using Electronic Design Automation (EDA) tools.

B. Fault Modeling and Injection

To generate labeled datasets, different fault models are introduced into the circuit:

- Stuck-at faults (SA0, SA1)
- Bridging faults
- Delay faults
- Transient faults

Faults are injected at different nodes using ATPG or fault simulation tools. The circuit response is recorded for both faulty and fault-free conditions. This step creates a structured dataset consisting of:

- Input test vectors
- Output responses
- Fault labels

C. Test Pattern Generation and Data Collection

Test patterns are generated using:

Automatic Test Pattern Generation (ATPG) tools Random test generators (RNG). These patterns are applied to the circuit, and corresponding outputs are collected. Each test case is labeled based on:

- Fault type
- Fault location

The collected dataset forms the foundation for training machine learning models.

D. Data Preprocessing and Feature Engineering

Raw circuit data is often high-dimensional and noisy. Therefore, preprocessing is performed:

- Data normalization and scaling
- Encoding of categorical values
- Removal of redundant data

Feature engineering techniques are applied to extract meaningful information:

- Statistical features (mean, variance)
- Signal transition patterns
- Switching activity

Dimensionality reduction techniques such as:

- Principal Component Analysis (PCA)
- Autoencoders are used to reduce computational complexity while preserving important information.

E. Machine Learning Model Development

In this stage, various machine learning models are developed and trained for fault classification:

1. Classical ML Models

- Support Vector Machine (SVM)
- Decision Tree Random Forest k-Nearest Neighbors (k-NN)

2. Deep Learning Models

- Artificial Neural Networks (ANN)
- Convolutional Neural Networks (CNN)

3. Graph-Based Models

Graph Neural Networks (GNN) for structural learning

The dataset is divided into:

- Training set
- Validation set
- Testing set

Hyperparameters are optimized using techniques such as cross-validation. Optimization algorithms like Stochastic Gradient Descent (SGD) and Adam are used for training.

F. Model Evaluation and Performance Metrics

The trained models are evaluated using standard performance metrics:

- Accuracy
- Precision
- Recall
- F1-score
- Confusion matrix

Additionally, system-level metrics include:

- Fault coverage
- Diagnosis resolution
- Computational complexity
- Training time

Comparative analysis is performed to identify the best performing model.

G. Fault Classification and Localization

The trained model is deployed to classify faults in unseen test data. The system performs:

- Fault detection (fault/no fault)
- Fault classification (type of fault)
- Fault localization (exact location in circuit)

This step enables faster and more accurate fault diagnosis compared to traditional approaches.

H. Deployment and Integration

The final stage involves integrating the trained model into real-world testing systems:

- Integration with ATPG tools
- Real-time fault detection systems
- Use in manufacturing test environments Advanced techniques include:
- Transfer learning for new circuit designs
- Reinforcement learning for adaptive test generation

The goal is to develop a scalable, adaptive, and intelligent fault detection system suitable for next-generation VLSI circuits.

Result

The proposed machine learning-based fault detection system for VLSI circuits demonstrates significant improvements over traditional testing methods. Experimental evaluation using benchmark datasets shows that classical machine learning models such as Support Vector Machines and Random Forest achieve high classification accuracy with relatively low computational cost. These models perform effectively on structured datasets generated through ATPG simulations, providing reliable fault detection for common fault types such as stuck-at faults. Furthermore, deep learning models, including Artificial Neural Networks and Convolutional Neural Networks, exhibit superior performance in handling complex and high-dimensional data, achieving higher accuracy and better generalization in large-scale circuits.

In addition, Graph Neural Networks show promising results in fault localization by effectively capturing the structural relationships within circuit topologies. The comparative analysis indicates that while deep learning and graph-based models provide higher accuracy, they require greater computational resources and larger training datasets. Overall, the proposed framework successfully reduces test time and improves fault detection efficiency compared to conventional methods. However, challenges such as scalability, real-time implementation, and dependency on labeled data remain. These results highlight the potential of integrating machine learning techniques into VLSI testing systems for developing intelligent, scalable, and efficient fault diagnosis solutions.

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Microsoft Windows [Version 10.0.26100.7623]
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C:\Users\KJ\Desktop\verilog>iverilog -o adder tb_adder4.v adder4.v

C:\Users\KJ\Desktop\verilog>vvp adder
A=0011 B=0101 SUM=01000
A=1111 B=0001 SUM=10000
A=1010 B=0101 SUM=01111
tb_adder4.v:22: $finish called at 43 (1s)

C:\Users\KJ\Desktop\verilog>iverilog -o adder_f tb_adder4_fault.v adder4_fault_sa0.v

C:\Users\KJ\Desktop\verilog>vvp adder_f
A=0011 B=0101 SUM=01000
A=1111 B=0001 SUM=10000
A=1010 B=0101 SUM=01110
tb_adder4_fault.v:23: $finish called at 30 (1s)

C:\Users\KJ\Desktop\verilog>
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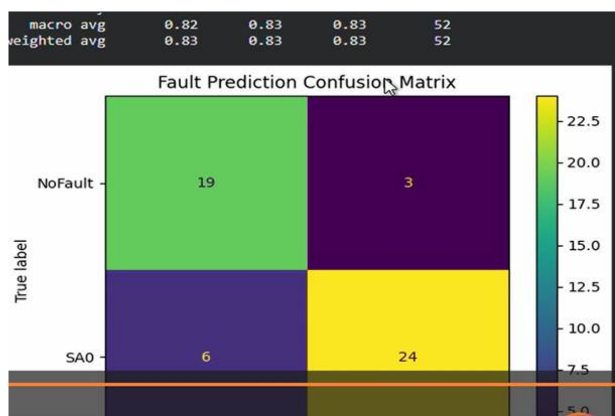

Conclusion

This research demonstrates that machine learning-based approaches offer a powerful and scalable solution for fault detection and localization in VLSI circuits, overcoming the limitations of traditional deterministic testing methods such as ATPG. By leveraging algorithms like Support Vector Machines, Random Forests, Artificial Neural Networks, and Graph Neural Networks, the proposed framework improves fault detection accuracy, reduces testing time, and enables

efficient handling of complex circuit structures. While classical machine learning models provide interpretability and efficiency for structured datasets, deep learning and graph-based techniques show superior performance in capturing nonlinear relationships and circuit topology. However, challenges such as high computational requirements, dependence on large, labeled datasets, and limited validation on real silicon remain significant barriers to practical deployment. Future work should focus on developing lightweight, adaptive, and real-time ML models, incorporating multiple fault types, and integrating with industrial EDA tools. Overall, this study highlights the potential of intelligent, data-driven methodologies in advancing reliable and efficient testing for next-generation VLSI systems.

References

1. Bushnell ML, Agrawal VD. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits. *Frontiers in Electronic Testing*. 2002;. Available from: 10.1007/b117406
2. Jha NK, Gupta S. Testing of Digital Systems. 2003;. Available from: 10.1017/cbo9780511816321
3. Goel P. An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits. *IEEE Transactions on Computers*. 1981;C-30(3):215-222. Available from: 10.1109/tc.1981.1675757
4. Wang LT, Wu CW, Wen X. *VLSI Test Principles and Architectures*. Morgan Kaufmann. 2006;. Available from: 10.1016/b978-012370597-6/50001-9
5. Huang Y, Abraham J. Algorithm-Based Fault Tolerance for Matrix Operations. *IEEE Transactions on Computers*. 1984;C-33(6):518-528. Available from: 10.1109/TC.1984.1676475
6. Breiman L. Random Forests. *Machine Learning*. 2001;45(1):5-32. Available from: 10.1023/a:1010933404324
7. Schapire RE. The Boosting Approach to Machine Learning. An Overview. *Nonlinear Estimation and Classification*. 2003;:149-171. Available from: 10.1007/978-0-387-21579-2_9
8. Mitra S, Kim KS. Machine learning applications in VLSI testing. *IEEE Design & Test*, vol. 34, no. 5, pp. 64–75, 2017.
9. Hinton GE, Salakhutdinov RR. Reducing the Dimensionality of Data with Neural Networks. *Science*. 2006;313(5786):504-507. Available from: 10.1126/science.1127647
10. LeCun Y, Bengio Y, Hinton G. Deep learning. *Nature*. 2015;521(7553):436-444. Available from: 10.1038/nature14539
11. Gaber L, Alzahrani AA, Gaddah MAA, Hammad A. Fault Detection based on Deep Learning for Digital VLSI Circuits. *Procedia Computer Science*. 2021;194:122-131. Available from: 10.1016/j.procs.2021.10.065
12. Moness M, Habib SMF, Hossain MA. Automated Design Error Debugging of Digital VLSI Circuits. *Journal of Electronic Testing*. 2022;38(4):395-417. Available from: 10.1007/s10836-022-06020-z
13. Wu Z, Pan S, Chen F, Long G, Zhang C, Yu PS. A Comprehensive Survey on Graph Neural Networks. *IEEE Transactions on Neural Networks and Learning Systems*. 2021;32(1):4-24. Available from: 10.1109/tnnls.2020.2978386
14. Hung SC, Hsu YC, Wen HM, Rutenbar RA. Graph Neural Network-based Delay-Fault Localization for Monolithic 3D ICs. *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. 2022;:448-453. Available from: 10.23919/date54114.2022.9774511
15. Shao S, Yu HY, Raghunathan A. Transferable Graph Neural Network-Based Delay-Fault Localization for Monolithic 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. 2023;42(11):4296-4309. Available from: 10.1109/tcad.2023.3275532
16. Wen X, Li P, Ying W. Machine learning-aided test pattern generation and optimization. *Proc. IEEE Design, Automation and Test in Europe (DATE)*, 2019.
17. Silver D, Huang A, Maddison CJ, Guez A, Sifre L, van den Driessche G, *et al*. Mastering the game of Go with deep neural networks and tree search. *Nature*. 2016;529:484-489. Available from: 10.1038/nature16961
18. Sutton RS, Barto AG. *Reinforcement Learning: An Introduction*, 2nd ed. MIT Press, 2018.
19. Tehranipoor M, Wang C. *Introduction to Hardware Security and Trust*. Springer. 2011;. Available from: 10.1007/978-1-4419-8080-9
20. Mitra S, Seifert N, Zhang M, Shi Q, Kim KS. Robust system design with built-in soft-error resilience. *Computer*. 2005;38(2):43-52. Available from: 10.1109/mc.2005.70
21. Javaid A, Tahir HR, Aslam M. Machine Learning Algorithms and Fault Detection for Improved Belief Function Based Decision Fusion in Wireless Sensor Networks. *Sensors*. 2019;19(6):1334. Available from: 10.3390/s19061334
22. Shaaban M, Eltawil AM, Fahmy HA. Deep learning for fault detection in integrated circuits: Advances and challenges. *IEEE Design & Test*, vol. 37, no. 5, pp. 33–41, 2020.
23. Mitra S, Kim KS. Diagnosis of intermittent and transient faults using data-driven techniques. *IEEE Design & Test*, vol. 35, no. 5, pp. 20–29, 2018.
24. El Sayed Z, Wang Z, Selmani H, Knechtel J, Sinanoglu O, Alrahis L. Graph Neural Networks for Integrated Circuit Design, Reliability, and Security: Survey and Tool. *ACM Computing Surveys*. 2026;58(4):1-44. Available from: 10.1145/3769081
25. Ali H, Khan T, Khan Z. Fault detection using machine learning-based dynamic independent component analysis. *Microelectronics Reliability*, vol. 150, 2024.
26. Moness M, Habib SMF. Semi-supervised deep learning models for VLSI fault detection. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 6, pp. 897–908, 2022.
27. Saha S, Siddiqui M. Machine learning-based fault detection framework for VLSI circuits using ATPG datasets. *Proc. International Conference on Emerging Technologies*, 2024.
28. Wen X, Li P, Ying W. Machine learning-aided test pattern generation and optimization. *Proc. IEEE DATE*, 2019.
29. Javaid A, Tahir HR, Aslam M. Machine Learning Algorithms and Fault Detection for Improved Belief Function Based Decision Fusion in Wireless Sensor Networks. *Sensors*. 2019;19(6):1334. Available from: 10.3390/s19061334
30. DfX-NYUAD. *GNN4IC: Graph neural networks for integrated circuits—A survey and benchmark collection*. GitHub Repository, 2024.
31. Data-driven fault localization in VLSI chips using semi-supervised learning. *International Journal of VLSI Design & Communication Systems*, vol. 16, no. 2, 2025.